WHAT IS CLAIMED IS:

1. A method of programming a memory cell that comprises a first transistor electrically connected to a second transistor, wherein said second transistor has a charge storage unit, comprising:

supplying a programming voltage to the cell;

providing a constant current between the first transistor and the second transistor;

generating hot electrons in the first transistor to charge the charge storage unit of the second transistor to a predetermined level; and

reducing hot electron generation, without changing the programming voltage or the constant current, in response to increasing charge level of the charge storage unit such that generation of hot electrons ceases, or substantially ceases, when the level of charge in the charge storage unit reaches within a margin of the predetermined level.

2. The method of claim 1 wherein the first transistor is controlled by a current mirror circuit having a reference current such that the current flowing between first transistor and the second transistor is controlled to be substantially equal to the reference current.

3. The method of claim 1 wherein said predetermined level of charge represents a binary logic state.

4. The method of claim 1 wherein said predetermined level of charge represents a multi-state logic state selected from a plurality of such logic states.

5. The method of claim 1 further comprising at least one step of ramping or pulsing a programming voltage to achieve a predetermined level of charge.

6. The method of claim 1 further comprising at least one step of verifying the charge of the charge storage unit.

7. The method of claim 1 further comprising at least one step supplying a voltage pulse to program

8. The method of claim 1 further comprising a plurality of programming and verifying steps.

9. A method of programming a memory cell that comprises a first transistor and a second transistor; said first transistor having a source, a drain, a channel region and a gate; said second transistor having a source, a drain, a channel region, a charge storage unit and a steering gate; the drain of the first transistor being electrically connected to the source of the second transistor; comprising:

applying a first fixed voltage to the drain of the second transistor;

applying a second fixed voltage to the steering gate of the second transistor;

controlling the voltage on the gate of the first transistor to produce a constant current between the drain of the first transistor and the source of the second transistor;

applying a data-dependant voltage to the source of the first transistor sufficient to initially produce hot electrons in the first transistor for programming the charge storage unit so that as the charge storage unit becomes charged hot electron production is reduced and charging of the charge storage unit is reduced.

10. The method of claim 9 wherein the data dependent voltage is applied to the source of the first transistor through a third transistor having a source, a drain, a channel region, a charge storage unit and a steering gate, the drain of the third transistor being connected to the source of the first transistor and the source of the third transistor being connected to the data dependent voltage; the method further comprising applying a voltage to the gate of the third transistor to produce a low impedance between the source and drain of the third transistor.

11. The method of claim 9 wherein the gate of the first transistor is connected to a wordline of a memory array.

12. The method of claim 9 wherein the drain of said second transistor is connected to a bitline of a memory array.

13. The method of claim 9 wherein the source of said third transistor is connected to a bitline of a memory array.

14. The method of claim 9 further comprising at least one step of either ramping a programming voltage, or applying data dependent voltage pulses to the source of the second transistor.

15. The method of claim 9 further comprising at least one step of verifying the charge level of the charge storage unit.

16. A programming circuit for programming a memory cell, the memory cell having two or more transistors electrically connected such that their channel regions are contiguous, comprising:

a current mirror circuit that forms a current mirror with a first transistor of the memory cell to provide a constant current through the first transistor of the memory cell; and

a data dependant voltage supply connected to said memory cell.

17. The programming circuit of claim 16 wherein the data dependant voltage is supplied to the first transistor.

18. The programming circuit of claim 16 wherein said current mirror circuit comprises:

a transistor that is substantially similar to the first transistor; and
a constant current source.

19. A method of charging a charge storage unit of a transistor to a target level, comprising:

producing hot electrons to charge the charge storage unit;

reducing the production of hot electrons in response to the charging of the charge storage unit such that hot electrons cease to be produced as the charge level approaches the target level.